CLAIMS

What is claimed is:

1. A method for performing a gather operation on a computer processor comprising:

computing addresses for one or more data elements of a matrix stored in memory;

loading each of said data elements into separate storage locations; and

depositing each of said data elements contiguously in a single storage location.

2. The method as in claim 1 wherein said storage locations are registers.

3. The method as in claim 1 wherein computing addresses comprises:

extracting indices for each of said data elements into separate storage locations; and

adding each of said indices to a base address.

4. The method as in claim 1 wherein depositing each of said data elements is accomplished via a DEPOSIT instruction executed by said computer processor.

5. The method as in claim 4 wherein said computer processor executes multiple DEPOSIT instructions in a single clock cycle.

6. The method as in claim 1 further comprising:

storing each of said data elements on a mass storage device.

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7. The method as in claim 2 wherein said registers are 64-bits wide and said data elements are 16-bits in length.

8. A method for performing a scatter operation on a computer processor comprising:

calculating addresses in memory to which a plurality of data elements are to be scattered to form a matrix in memory;

extracting each of said data elements from a storage location in which said elements are stored contiguously; and

storing said data elements to said addresses in memory.

9. The method as in claim 8 wherein said storage location is a register.

10. The method as in claim 8 wherein computing addresses comprises:

extracting indices for each of said data elements into separate storage locations; and

adding each of said indices to a base address.

11. The method as in claim 8 wherein extracting each of said data elements is accomplished via an EXTRACT instruction executed by said computer processor.

12. The method as in claim 11 wherein said computer processor executes multiple EXTRACT instructions in a single clock cycle.

13. The method as in claim 9 wherein said register is 64-bits wide and said data elements are 16-bits in length.

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14. A computer system comprising:

a memory;

a processor communicatively coupled to the memory; and

a storage device communicatively coupled to the processor and having stored therein a sequence of instructions which, when executed by the processor, causes the processor to at least,

compute addresses for one or more data elements of a matrix stored in memory;

load each of said data elements into separate storage locations; and

deposit each of said data elements contiguously in a single storage location.

15. The computer system as in claim 14 wherein said storage locations are registers.

16. The computer system as in claim 14 wherein, responsive to one or more instructions in said sequence, said processor computes addresses by:

extracting indices for each of said data elements into separate storage locations; and

adding each of said indices to a base address.

17. The computer system as in claim 14 wherein depositing each of said data elements is accomplished via a DEPOSIT instruction executed by said processor.

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18. The computer system as in claim 17 wherein said processor executes multiple DEPOSIT instructions in a single clock cycle.

19. The computer system as in claim 14 wherein, responsive to one or more instructions in said sequence, said processor further:

stores each of said data elements on said mass storage device.

20. The computer system as in claim 15 wherein said registers are 64-bits wide and said data elements are 16-bits in length.

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